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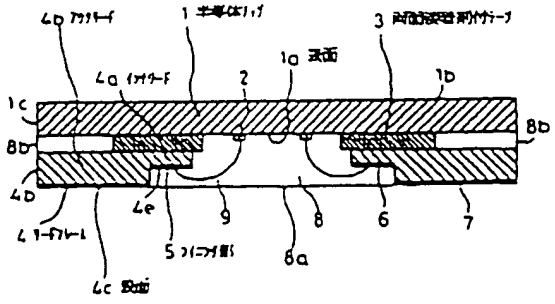
(54)【発明の名称】半導体装置

(57)【要約】
【課題】半導体チップの上に同一サイズのリードフレームを載せるＣＳＰ（ChipScale Package）構造において、パッケージ厚さをより薄くする。
【解決手段】半導体チップ１に貼り付けるリードフレーム４は、半導体チップ１と略同一サイズとする。リードフレーム４のインナリード４ａの表面４ｅにコイニングを施して厚みを減らしたコイニング部５を形成する。両面絶縁樹付テープ３を介してリードフレーム４と半導体チップ１とを裏面４ｄ、１ｃを合わせて貼り付ける。インナリード４ａのコイニング部５と半導体チップ１のボンディングパッド２とをボンディングワイヤ９で接続する。半導体チップ１の表面１ａにモールド樹脂８を封止し、封止樹脂表面８ａにアウタリード４ｂの表面４ｃのみを露出させる。



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【特許請求の範囲】

【請求項１】半導体チップの表面に半導体チップと略同一サイズのリードフレームを重ね合わせて接着剤を介して貼り付け、リードフレームのインナリードと半導体チップとをボンディングワイヤで接続し、アウタリードの表面と面一となるように半導体チップの表面側をモールド樹脂で封止して、封止樹脂表面にアウタリードの表面を露出させた半導体装置において、インナリードに接続されるボンディングワイヤがアウタリードの表面を越えないように、インナリードの表面側の厚みを減らしてインナリード表面をアウタリード表面より一段低くしたことを特徴とする半導体装置。

【請求項２】上記リードフレームのサイズを半導体チップよりやや大きめに形成し、該リードフレームを半導体チップの表面に重ね合わせたとき形成される端面間のギャップもモールド樹脂で封止するようにした請求項１に記載の半導体装置。

【請求項３】上記半導体チップの表面にリードフレームを貼り付ける接着剤を、インナリード側のみならずアウタリード側にも介在させた請求項１または２に記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はリードフレームを使用した半導体装置に係り、特にチップサイズと略同一のサイズをもつ薄型かつ小型の半導体パッケージ構造に関するものである。

【０００２】

【従来の技術】大容量のＤＲＡＭ（Dynamic Random Access Memory）では、高密度実装の要求に対応して、比較的小さなパッケージに大形化した半導体チップを収納できるＬＯＣ（Lead On Chip）構造が採用されているが、容量の増加により更にチップサイズレベルにまで小形化されたパッケージが要求されるようになってきた。また、電子機器用の半導体パッケージも、パソコン、ファックス、パーソナル電話機、ＩＣカード等のサイズの縮小に伴って、より小形化することが要求されている。しかも、この小形化は、単にパッケージの専有する面積にのみ求められるのではなく、パッケージの厚さ方向にも求められている。

【０００３】従来、これらの要請に応えるものとして、リードの一部のみをパッケージの底面に露出させたＣＳＰ（Chip Scale Package）と呼ばれる半導体装置が提案されている（特開平６－１３２４５３号公報）。具体的には、図７に示すように、半導体チップ２１の配線面（表面）２１ａに半導体チップ２１と同一サイズのリードフレーム２２を端面を合わせて接着剤２３で貼り付ける。リードフレーム２２のインナリード２２ａと半導体チップ２１とをボンディングワイヤ２４で接続した後、モールド樹脂２５で封止する際、半導体チップ２１の表面側をモールド樹脂２５で封止して、モールド樹脂２５の表面２５ａにアウタリード２２ｂの表面２２ｃを露出させたものである。

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【０００４】ここに、インナリード２２ａと半導体チップ２１とを接続するボンディングワイヤ２４が、アウタリード２２ｂの表面２２ｃと面一にしたモールド樹脂２５の表面２５ａからはみださないように、リードに段差を設ける必要があるが、この従来例では、リードフレーム２２をダウンセット加工することによって、インナリード２２ａをアウタリード２２ｂよりも一段低くしている。

【０００５】

【発明が解決しようとする課題】上述した従来技術によって、パッケージの小形化は、パッケージの専有する面積に反映されるばかりでなく、パッケージの厚さ方向にも反映されるようになってきた。しかし、リードフレームをダウンセット加工することによってリードに段差を設けるようにしているので、リード厚を超えた加工深さが必要となり、その分、パッケージ厚さを薄くできない。

【０００６】また、パッケージのサイズが半導体チップ１と同一であると、最小のパッケージを得ることができるが、半導体チップ１の大きさのばらつきによっては、モールド樹脂封止時にモールド金型が半導体チップ１の一部を破損してしまうおそれがある。

【０００７】さらに、半導体チップへのリードフレームの接着固定は、インナリード側のみで行なっているため、モールド樹脂封止の際に、アウタリード側の厚み方向での固定が十分でない場合が生じるが、固定が十分でないと、アウタリードの表面にモールド樹脂が薄く回り込み、表面を削り出す必要があった。

【０００８】本発明の目的は、上述した従来技術の問題点を解消して、パッケージ厚さをより薄くできる半導体装置を提供することにある。また、本発明の目的は、モールド樹脂封止時、半導体チップが破損しない半導体装置を提供することにある。さらに、本発明の目的は、モールド樹脂封止後、アウタリード表面の削り出しを必要としない半導体装置を提供することにある。

【０００９】

【課題を解決するための手段】本発明の半導体装置は、半導体チップの表面に半導体チップと略同一サイズのリードフレームを重ね合わせて接着剤を介して貼り付け、リードフレームのインナリードと半導体チップとをボンディングワイヤで接続し、アウタリードの表面と面一となるように半導体チップの表面側をモールド樹脂で封止して、封止樹脂表面にアウタリードの表面を露出させた半導体装置において、インナリードに接続されるボンディングワイヤがアウタリードの表面を越えないようにインナリードの表面側の厚みを減らしてインナリード表面をアウタリード表面より一段低くしたものである。こ

のようにインナリードの厚みをアウタリードよりも減らしてインナリードをアウタリードより一段低くできるようにすると、リードをダウンセットする場合に比して、パッケージ厚さをより薄くすることができる。

【００１０】また、このような本発明の半導体装置において、リードフレームのサイズを半導体チップよりやや大きめに形成し、リードフレームを半導体チップの表面に重ね合わせたとき形成される端面間のギャップもモールド樹脂で封止することが、半導体チップの破損を有効に防止できる。また、半導体チップの表面にリードフレームを貼り付ける接着剤を、インナリード側のみならずアウタリード側にも介在させることが、アウタリードの表面へのモールド樹脂の回り込みを防止できる。

【００１１】

【発明の実施の形態】以下に本発明の半導体装置の実施の形態を図面を用いて詳細に説明する。図１は、半導体チップ１上に同一サイズのリードフレーム４を載せたＣＳＰ構造の断面図である。

【００１２】半導体チップ１は、その配線面である表面１ａの中央近傍にボンディングパッド２が配置されて構成される。この半導体チップ１の表面１ａに貼り付けられるリードフレーム４は、半導体チップ１と同一サイズで構成され、半導体チップ１と接続するためのインナリード４ａと、外部端子となるアウタリード４ｂとを有する。半導体チップ１とリードフレーム４との貼付けは、半導体チップ１の端面１ｃとリードフレーム４の端面４ｄとが一致するように、半導体チップ１とリードフレーム４とを重ね合わせて、両面接着剤付テープ３を介して行う。

【００１３】リードフレーム４は折曲していない代りに、一部の厚さを減らして薄くしてある。すなわち、リードフレーム４のインナリード４ａは、その貼付け面と反対面（表面４ｅ）側をコイニングしてアウタリード４ｂよりも薄くしたコイニング部５を形成し、インナリード４ａと半導体チップ１のボンディングパッド２とを接続するボンディングワイヤ９の高さをアウタリード４ｂの貼付け面と反対面（表面４ｃ）よりも低くなるようにしてある。

【００１４】このようにして厚さを減らしてアウタリード４ｂの表面４ｃよりも一段低くしたインナリード４ａのコイニング部５には細めっき６が施され、細めっき６が施されたコイニング部５と半導体チップ１の中央近傍に配されたボンディングパッド２とがボンディングワイヤ９によって接続される。コイニング部５が一段低くなっているため、ボンディングワイヤ９の高さは、アウタリード４ｂの表面４ｃより低く抑えることができる。

【００１５】モールド樹脂８による封止は、半導体チップ１の表面１ａ側で行なわれる。モールド樹脂８の厚さを　アウタリード４ｂの表面４ｃと同一高さにして、インナリード４ａおよびボンディングワイヤ９などをモールド樹脂８中に埋めて保護するが、アウタリード４ｂの表面４ｃは封止樹脂表面８ａに露出させる。このとき、パッケージの面積を小さく、かつパッケージの厚さを薄くするために、モールド樹脂８は、リードフレーム４の端面４ｄ及び半導体チップ１の端面１ｃ及び半導体チップ１の裏面１ｂに回りこまないようにする。

【００１６】このように構成された半導体パッケージは、コイニングによってリードに段差を設けているため、従来のようにリードフレームをダウンセットする必要はない。また、パッケージ厚さは半導体チップ厚、両面接着剤付テープ厚、及び１枚のリード厚を合計した厚さとなり、ダウンセットが要求するリード厚の２倍以上の加工厚さがリード部分に要求されないため、パッケージの厚さをより薄くすることができる。

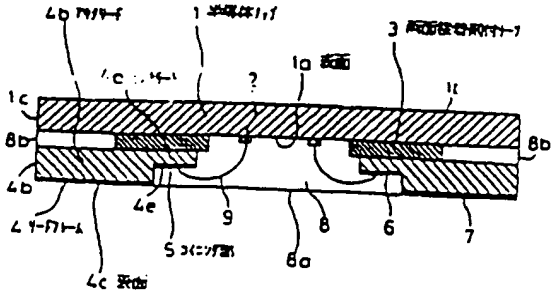
【００１７】上述した半導体パッケージを製造するには、まず、モールド樹脂８の端面８ｂを半導体チップ１の端面１ｃに一致させるために、パッケージに使用されるリードフレーム４は、その樹脂ダムバー１７の位置を、図２に示すように、一点鎖線で示した半導体チップ１の外周に沿って配置するように構成する。また、パッケージ製造時に使用するモールド金型は、半導体チップ１の外形とほぼ同じ大きさとし、半導体チップ１の裏面１ｂ側にモールド樹脂８が回らないようにして、半導体チップの表面側のみをモールドする。なお、リードフレーム４の端面４ｄは樹脂ダムバー１７の切断面となる。

【００１８】モールド後、樹脂ダムバー１７を金型で切断し、リード４ａ、４ｂを個々に切り離す。ここで、樹脂ダムバー１７を切断する前に、モールド樹脂８の表面８ａに露出するアウタリード４ｂの表面４ｃに、半田との濡れが良好な細めっき７をインナリード４ａのコイニング部５の細めっき６と同時に行っておくのがよい。こうするとアウタリード４ｂの表面の外装半田めっきは不要となり、コスト低減できるとともに、モールド後、パッケージにダメージを与える工程を減らすことができる点でも有利である。

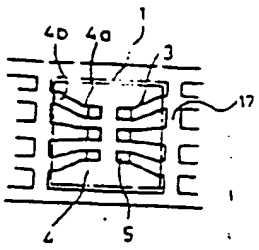
【００１９】本製造方法によれば、従来より行われているＬＯＣリードフレームの製造工程、および樹脂モールド工程をそのまま、または、一部省略して利用することができるため、従来のモールドパッケージと比較して価格的に同等でありながら、より小型かつ薄型のパッケージを得ることができる。

【００２０】ところで、図１に示すパッケージ構造のモールド領域では、パッケージのサイズが半導体チップ１と同一であるため、半導体チップ１の大きさのばらつきによっては、モールド金型が半導体チップ１の一部を圧接してしまうことが懸念される。このような懸念は、図３に示すように、半導体チップ１に対してモールド領域を若干拡大する設定を行うことよって解消できる。すなわち、リードフレーム４のサイズを半導体チップ１よりやや大きめに形成し、このやや大きめに形成したリード

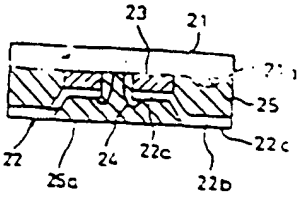
【図１】



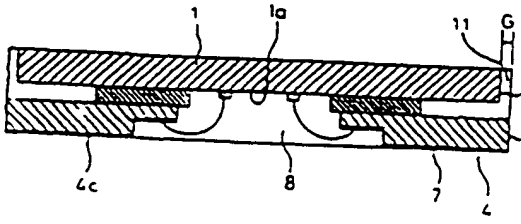
【図２】



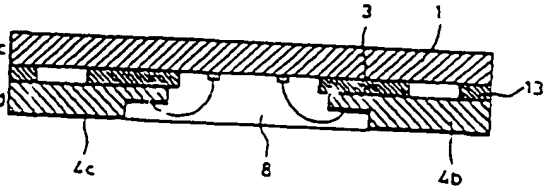
【図７】



【図３】



【図４】



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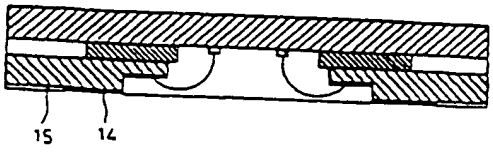
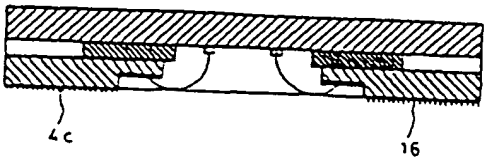


【図６】



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Japanese Patent Laid-Open Publication No. Heisei 9-92775

[TITLE OF THE INVENTION]

Semiconductor Device

[CLAIMS]

1. A semiconductor device including a semiconductor chip, a lead frame having a size substantially equal to that of the semiconductor chip, the lead frame being bonded to a surface of the semiconductor chip by an adhesive layer interposed therebetween under the condition in which the lead frame is overlapped with the semiconductor chip, bonding wires adapted to bond inner leads included in the lead frame to the semiconductor chip, and a resin encapsulate adapted to encapsulate a region toward the surface of the semiconductor chip in such a fashion that it has a surface flush with a surface of each of outer leads included in the lead frame to expose the surface of the outer lead at the surface of the resin encapsulate, wherein each of the inner leads has a reduced thickness at a surface thereof in such a fashion that the bonding wire connected to the inner lead does not extend beyond the surface of an associated one of the outer leads, whereby the surface of the inner lead is lower than the surface of the outer lead by one step.

2. The semiconductor device in accordance with claim 1, wherein the size of the lead frame is slightly larger than that of the semiconductor chip, and the resin encapsulate fills a gap defined between corresponding end surfaces of the semiconductor chip and the lead frame when the lead frame is laid on the surface of the semiconductor chip in an overlapped state.

3. The semiconductor device in accordance with claim 1 or 2, wherein the adhesive layer is disposed not only at a region where the inner leads are arranged, but also at a region where the outer leads are arranged.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a semiconductor device using a lead frame, and more particularly to a semiconductor package having a thin and compact structure substantially equal in size to a semiconductor chip packaged therein.

[DESCRIPTION OF THE PRIOR ART]

In DRAMs (Dynamic Random Access Memories) having a large capacity, an LOC (Lead On Chip) structure is mainly

used which is capable of allowing a semiconductor chip having a large size to be packaged in a relatively small package, in order to meet a requirement of high-density mounting. However, the recent demand of an increased capacity has resulted in a requirement of compact semiconductor packages having a size reduced to a chip size level. Similarly, semiconductor packages for electronic appliances such as facsimile machines, personal computers, IC cards, and the like has been required to have a more compact structure in pace with the recent trend of those electronic appliances toward a compactness. Furthermore, such a compactness of a semiconductor package have been required with regard to not only the area occupied by the semiconductor package, but also the thickness of the semiconductor package.

In order to meet such requirements, a semiconductor device has been proposed which is called a "CSP (Chip Scale Package)" (Japanese Patent Laid-open Publication No. Heisei 6-132453). In such a CSP package, each lead is partially exposed at the lower surface of the package. Referring to Fig. 7 illustrating a detailed structure of this CSP package, a lead frame 22 having the same size as that of a semiconductor chip 21 is bonded to the wiring surface of the semiconductor chip 21, that is, the surface 21a, in such a fashion that their corresponding edges are aligned

with each other, by means of an adhesive 23. Inner leads 22a of the lead frame 22 are connected to the semiconductor chip 21 by means of bonding wires 24. In this state, an encapsulating process is carried out using a molding resin 25. In this encapsulating process, the semiconductor chip 21 is encapsulated by the molding resin 25 at its portion toward its surface 21a, thereby causing the surface 22c of each outer lead 22b to be exposed at the surface 25a of the molding resin 25.

In this case, it is necessary to provide a stepped lead structure in order to prevent the bonding wires 24 serving to connect the inner leads 22a to the semiconductor chip 21 from being protruded from the surface 25a of the resin 25 flush with the surfaces 22c of the outer leads 22b. To this end, in this conventional example, the lead frame 22 is subjected to a down-setting process so that each inner lead 22a is lower than an associated one of the outer leads 22c by one step.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

In accordance with the above mentioned conventional technique, compactness of a semiconductor package can be achieved with regard to not only the area occupied by the semiconductor package, but also the thickness of the semiconductor package. However, since this technique

provides a stepped lead structure by down-setting the lead frame, it requires a machining depth exceeding the lead thickness. For this reason, it is impossible to produce a package having a thickness less than the machining depth.

Where the semiconductor chip 1 has the same size as that of a package to be produced, the package may have a minimized size. However, if the semiconductor chip 1 has a non-uniform size, it may be damaged by a mold during an encapsulating process using the molding resin.

Furthermore, the lead frame may be in a state insufficiently fixed in a thickness direction at its portion near the outer leads during the encapsulating process because the bonding and fixing of the lead frame to the semiconductor chip is achieved at a portion of the lead frame near the inner leads. As a result, the molding resin may spread in the form of a thin film on the outer lead surface. In this case, it is necessary to shave off the resin film coated on the outer lead surface.

An object of the invention is to solve the above mentioned problems involved in the prior art, and to provide a semiconductor device having a reduced package thickness. Another object of the invention is to provide a semiconductor device having a structure capable of preventing its semiconductor chip from being damaged during an encapsulating process using a molding resin. Another

object of the invention is to provide a semiconductor device having a structure capable of eliminating a requirement for its outer lead surface to be shaved off after an encapsulating process.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

The present invention provides a semiconductor device including a semiconductor chip, a lead frame having a size substantially equal to that of the semiconductor chip, the lead frame being bonded to a surface of the semiconductor chip by an adhesive layer interposed therebetween under the condition in which the lead frame is overlapped with the semiconductor chip, bonding wires adapted to bond inner leads included in the lead frame to the semiconductor chip, and a resin encapsulate adapted to encapsulate a region toward the surface of the semiconductor chip in such a fashion that it has a surface flush with a surface of each of outer leads included in the lead frame to expose the surface of the outer lead at the surface of the resin encapsulate, wherein each of the inner leads has a reduced thickness at a surface thereof in such a fashion that the bonding wire connected to the inner lead does not extend beyond the surface of an associated one of the outer leads, whereby the surface of the inner lead is lower than the surface of the outer lead by one step.

In the semiconductor device of the present invention, the size of the lead frame may be slightly larger than that of the semiconductor chip. In this case, the resin encapsulate fills a gap defined between corresponding end surfaces of the semiconductor chip and the lead frame when the lead frame is laid on the surface of the semiconductor chip in an overlapped state. Accordingly, it is possible to effectively prevent the semiconductor chip from being damaged. The adhesive layer may be disposed not only at a region where the inner leads are arranged, but also at a region where the outer leads are arranged. In this case, it is possible to prevent the molding resin from spreading on the outer lead surface.

[PREFERRED EMBODIMENTS OF THE INVENTION]

Hereinafter, preferred embodiments of the present invention will be described in detail in conjunction with the annexed drawings. Fig. 1 is a cross-sectional view illustrating a CSP structure in which a lead frame 4 having the same size of a semiconductor chip 1 is bonded to the semiconductor chip 1.

The semiconductor chip 1 is provided at its wiring surface, namely, a surface 1a, with bonding pads 2. These bonding pads 2 are arranged in the vicinity of the central portion of the surface 1a. The lead frame 4, which is

attached to the surface 1a of the semiconductor chip 1, has the same size as that of the semiconductor chip 1. The lead frame 4 includes inner leads 4a adapted to come into contact with the semiconductor chip 1, and outer leads 4b each serving as an external terminal. The attachment between the semiconductor chip 1 and lead frame 4 is achieved by overlapping the semiconductor chip 1 and lead frame 4 with each other in such a fashion that each end surface 1c of the semiconductor chip 1 is aligned with an associated one of end surfaces 4d of the lead frame 4, and interposing a double-sided adhesive tape 3 between the overlapped semiconductor chip 1 and lead frame 4.

The lead frame 4 has a structure not bent, but having a reduced thickness at a desired portion thereof. That is, each inner lead 4a has a coining portion 5 having a thickness less than that of an associated one of the outer leads 4b. The coining portion 5 is formed by coining a surface of the inner lead 4a opposite to the bonding surface of the inner lead 4a, that is, a surface 4c. Accordingly, bonding wires 9, which connect the inner leads 4a to bonding pads 2 of the semiconductor chip 1 respectively, have a height lower than a surface of each outer lead 4b opposite to the bonding surface of the outer lead 4b, that is, the surface 4c.

For the coining portion 5 of each inner lead 4a

arranged at a level lower than the surface 4c of the associated outer lead 4b by virtue of the above mentioned thickness reduction, a silver plating process is conducted to form a silver plating film 6. The coining portions 5 formed with the silver plating films 6 are connected with the bonding pads 2 arranged near the central portion of the semiconductor chip 1 by means of the bonding wires 9, respectively. Since each coining portion 5 is arranged at a level lower than the surface 4c of the associated outer lead 4b by one step, the associated bonding wire 9 can be controlled to have a height lower than the surface 4c of the outer lead 4b.

An encapsulating process using a molding resin is conducted at a region toward the surface 1a of the semiconductor chip 1, thereby forming a resin encapsulate 8. The thickness of the resin encapsulate 8 is determined in such a fashion that the resin encapsulate 8 is flush with the surfaces 4c of the outer leads 4b at its surface 8a. The inner leads 4a and bonding wires 9 are encapsulated by the resin encapsulate 8 so that they are protected. The surfaces 4c of the outer leads 4b are exposed at the surface 8a of the resin encapsulate 8. In order to reduce the area of the package while reducing the thickness of the package, the resin encapsulate 8 is prevented from extending beyond each end surface 4d of the

lead frame 4, each end surface 1c of the semiconductor chip 1c, and the surface 1b of the semiconductor chip 1.

Since the semiconductor package configured as mentioned above has a stepped lead structure formed using a coining process, it is unnecessary for its lead frame to be down-set. The semiconductor package has a thickness corresponding to the sum of the thickness of the semiconductor chip, the thickness of the double-sided adhesive tape, and the thickness of one lead sheet. The thickness of the semiconductor package can be minimized because the lead portion of the semiconductor package involves no machining depth, corresponding to at least two times the lead thickness, required in a down-set structure.

In the fabrication of the above mentioned semiconductor package, the lead frame 4 used to fabricate the semiconductor package is arranged with respect to the semiconductor chip 1 in such a fashion that its resin dam bars 17 extend along the peripheral edges of the semiconductor chip 1 indicated by dotted lines in Fig. 2, so as to align each end surface 8b of the resin encapsulate 8 with the associated end surface 1c of the semiconductor chip 1. The mold used in the fabrication of the semiconductor package has a size substantially equal to the size of the semiconductor chip 1. The resin encapsulate 8 is molded only at a region toward the surface 1a of the

semiconductor chip 1 while being prevented from spreading on the surface 1b of the semiconductor chip 1. Each resin dam bar 17 is cut along the associated end surface 4d of the lead frame 4.

After molding, the resin dam bars 17 are cut from the mold, thereby achieving a separation of the leads 4a and 4b. It is desirable that, prior to the cutting of the resin dam bars 17, a silver plating film 7 providing a good flowability of solder is formed on the surfaces 4c of the outer leads 4b exposed at the surface 8a of the resin encapsulate 8. The formation of the silver plating film 7 may be conducted simultaneously with the formation of the silver plating film 6 on the coining portions 5 of the inner leads 4a. In this case, it is unnecessary to conduct an external solder plating process for the surfaces of the outer leads 4b. Accordingly, it is possible to reduce the costs. Also, there is an advantage in that the number of processes, which may damage the package after the completion of the molding process, is reduced.

In accordance with the fabrication method according to the present invention, it is possible to use the fabrication process for LOC lead frames and the resin molding process associated therewith as they are or while partially eliminating them. Therefore, it is possible to obtain a package having a more compact and thinner

structure while being equivalent in costs, as compared to conventional molded packages.

In the semiconductor package structure shown in Fig. 1, however, if the semiconductor chip 1 has a deviation in size, the mold may then damage a part of the semiconductor chip 1. This is because the package has the same size as the semiconductor chip 1 at its molding region. Such a problem can be eliminated by setting the molding region to have a size slightly larger than that of the semiconductor chip 1. Where the lead frame 4 is fabricated to have a size slightly larger than that of the semiconductor chip 1, and the mold is constructed to have a size corresponding to a region defined by the resin dam bars 17 defining the slightly increased size of the lead frame 4, the mold does not come into contact with the end surfaces 1c of the semiconductor chip 1 even when the semiconductor chip 1 has a deviation in size. Accordingly, it is possible to prevent the semiconductor chip 1 from being damaged. Although there is a gap G defined between each end surface 4d of the lead frame 4 and the associated end surface 1c of the semiconductor chip 1, this gap G is filled with the molding resin 11 during the formation of the resin encapsulate 8. Thus, the end surfaces 1c of the semiconductor chip 1 are protected by the mold resin 11 after the formation of the resin encapsulate 8.

Furthermore, in the semiconductor package structure shown in Figs. 1 and 3, if the lead frame is in a state insufficiently fixed in a thickness direction at its portion near the outer leads 4b by the double-sided adhesive tape 3 arranged at the inner lead region during the encapsulating process, the molding resin may spread in the form of a thin film on the surface 4c of the outer leads 4b. In this case, it is necessary to shave off the resin film coated on the surface 4c. The phenomenon of the molding resin spreading on the outer lead surface 4c can be effectively prevented by interposing a double-sided adhesive tape 13 having the same thickness as the double-sided adhesive tape 3 between the semiconductor chip and the outer leads 4b in the vicinity of the periphery of the package. A combination of the structures shown in Figs. 3 and 4 may also be used.

Although the silver plating film 7 is formed over the entire portion of the surface 4c of each outer lead 4b in the structure of Fig. 1, 3 or 4, this may inevitably result in an increase in costs because of an increase in the amount of silver used. However, the amount of silver used can be reduced by reducing the area coated with the silver plating film, as indicated by the reference numeral 14 in Fig. 5. In this case, there is an advantage in regard to costs. The reference numeral 15 denotes an area plated

with no silver plating film.

Fig. 6 illustrates an example in which a solder plating film 16 is formed on the surface 4c of each outer lead 4b. As described above, the formation of the solder plating film on the surface of the outer lead 4b inevitably involves an increase in the number of processes damaging the package. Of course, this is not avoided in the present invention.

In the above mentioned embodiment of the present invention, a semiconductor chip was used which has a thickness of 0.3 mm. The lead frame used has a thickness of 0.15 mm. Also, the double-sided adhesive tape has a total thickness of 0.05 mm. The inner leads were subjected to a coining process to have coining portions having a thickness of 0.075 mm. Although the coining process was used as a method for reducing the thickness of the inner leads, a half-etching process may be used. Although the double-sided adhesive tape was used as a means for attaching the semiconductor chip to the lead frame, an adhesive may be simply used.

[EFFECTS OF THE INVENTION]

In accordance with the present invention, a stepped lead structure is provided by a reduction in the thickness of each inner lead. Accordingly, it is unnecessary to give a machining depth exceeding the lead thickness. Such a machining depth is required in the conventional method in

which a stepped lead structure is provided in accordance with a down-setting process. Thus, it is possible to produce a semiconductor package having a reduced thickness. Since the lead frame has a size slightly larger than that of the semiconductor chip in accordance with the present invention, it is possible to effectively prevent the semiconductor chip from being damaged by the mold.

Moreover, it is possible to prevent the molding resin from spreading on the surfaces of the outer leads because the adhesive adapted to bond the lead frame to the surface of the semiconductor chip is also applied to the outer leads. Accordingly, it is unnecessary to shave off the outer lead surfaces.